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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,013	07/08/2003	Kee-Won Kwon	SEC.1032	9516

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,013	KWON ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,9-11* is/are rejected.

7)☒ Claim(s) *6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on July 8, 2003.

2. Claims 1 – 11 are pending in this case. Claims 1 and 10 are independent claims.

Preliminary Amendment

3. Acknowledgment is made of applicant's Preliminary Amendment, filed July 8, 2003. The changes and remarks under Specification on page 12, paragraph [00057] disclosed therein were considered.

Specification

4. Content of Specification

(e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(f) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may

> point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

The disclosure is objected to because of the following informalities: Need to separate BACKGROUND and SUMMARY into its own paragraph.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-5 and 9-11 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding independent claim 1, Fig. 4 of AAPA discloses a semiconductor memory device in which a plurality of memory cells are arranged in the form of a matrix in row and column directions (page 1 paragraph 0019), the semiconductor memory device comprising: a plurality of memory array blocks [21's] each including set numbers of memory cells (21's, each 21 having 3 sub-blocks of memory cells), the memory array blocks being arranged in the row direction (page 1 paragraph 0019); a Row Address Strobe (RAS) chain [23] aligned at a first side of the plurality of memory array blocks in

the row direction, the RAS chain selecting and activating a particular word line (page 2 paragraph 0020); a Column Address Strobe (CAS) chain aligned at a second side of the plurality of memory array blocks in the column direction, the CAS chain for amplifying N bits (8-bit data lines) of data from the plurality of memory array blocks (page 2 paragraph 0021), and outputting the result to an input/output (IO) line (8-bit lines), wherein N (8) is a natural number more than 2; and a data converter [25] for (25, page 2 paragraph 0022 disclosing 8-bit data is converting to serial data) continuously outputting the N bits of data input via the IO line from a memory array block [21] nearest (the most left of memory block 21) to the RAS chain [23] to a memory array block farthest from the RAS chain (the most right of memory block 21).

Regarding dependent claim 2, Fig. 4 of AAPA further discloses wherein: the plurality of memory array blocks [21's] are arranged with respect to the RAS chain in the order of a first memory block, a second memory bock, ..., and an Mth memory array block (left to right of memory block 21's), so that the first memory array block is nearest (the most left block of 21's) to the RAS chain [23] and the Mth memory array block is farthest (the most right block of 21) from the RAS chain [23], and the data converter [25] converts the N bits of data output from the first, second, and the Mth memory array block into a first bit, a second bit, ..., an Mth bit of N data pins, respectively, and outputs the result in the order from the first bit to the Mth bit (DQ7 - - - DQ0).

Regarding dependent claim 3, Fig. 4 of AAPA discloses wherein the data converter may be a shift register and includes the functions of a multiplexer (25 [MUX]).

Regarding dependent claim 4, Fig. 4 of AAPA further discloses wherein the respective memory array blocks are divided into predetermined numbers of memory sub-blocks (3 sub-blocks 22 for each memory block 21).

Regarding dependent claim 5, AAPA discloses wherein the nearer a memory array block comes to the RAS chain, the greater the number of the memory sub-blocks of the memory array block (Fig. 4).

Regarding dependent claim 9, Fig. 4 of AAPA discloses wherein the nearer a memory array block [21] comes to the RAS chain (right to left of memory blocks 21's), the greater the number of the memory sub-blocks [22] of the memory array block.

Regarding independent claim 10, Fig. 4 of AAPA discloses a semiconductor memory device in which a plurality of memory cells (paragraph 0019) are arranged in the form of a matrix in row and column directions, the semiconductor memory device comprising: a plurality of memory array blocks [21's] including predetermined numbers of memory cells (inherent to memory blocks 21's, because memory block is formed by predetermined number of memory cells), the memory array blocks being arranged in the row direction (Fig. 4), a Row Address Strobe (RAS 23) chain arranged at a first side of the plurality of memory array blocks in the row direction, the RAS chain for selecting and activating a particular word line (paragraph 0020); a Column Address Strobe (CAS 24) chain arranged at a second side of the plurality of memory array blocks in the column direction (Fig. 4), the CAS chain for amplifying N bits of data output (8-bit data lines) from the plurality of memory array blocks (21's, page 2 paragraph 0021) and outputting the amplified N bits of data to an I0 line (8-bit lines), wherein N (8) is a natural

number more than 2; and a plurality of multiplexers (25's) for converting the N bits of data input via the I0 line into serial data and outputting the serial data (25, page 2 paragraph 0022 disclosing 8-bit data is converting to serial data), wherein the respective memory array blocks are divided into predetermined numbers of memory sub-blocks (23), and the nearer a memory array block is to the RAS chain (the most left block 21 of Fig. 4), the smaller the number of the memory sub-blocks (3) of the memory array block [21's].

Regarding dependent claim 11, AAPA discloses wherein the respective memory array blocks substantially output N bits of data at the same point of time (page 2 first two lines of paragraph 0023 disclosing the DQ0 through DQ7 bits data must be input output in response to the same clock).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being anticipated by Applicant Admitted Prior Art (AAPA), in view of Kawamura U.S. Patent No. 5,485,424

Fig. 4 of AAPA as applied to claim 1 above discloses every aspect of applicant's claimed invention except for wherein: the plurality of memory array blocks further comprise a plurality of redundancy memory array blocks, and each of the plurality of

redundancy memory array blocks is arranged to have a data I0 path through which data is input and output to be the same as or be faster than those to I0 paths of memory array blocks, and the memory array blocks are repaired by the redundancy memory array blocks.

Fig. 5 of Kawamura discloses a memory array blocks [1] having a redundancy memory block the plurality of memory array blocks further comprise a plurality of redundancy memory array blocks [3, 18], and each of the plurality of redundancy memory array blocks is arranged to have a data I0 path through which data is input and output to be the same as or be faster than those to I0 paths of memory array blocks (Col. 3 lines 12 – 17 disclosing a redundancy circuit memory having access speed comparable to access speed of normal memory cell. Since "comparable" means the same or greater than or less than, therefore "comparable" to speed taught by Kawamura is read on "faster or same" of the invention), and the memory array blocks are repaired by the redundancy memory array blocks (repairing memory cell is a inherency function of redundancy memory).

AAPA and Kawamura are common subject matter of semiconductor memory device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the redundant memory circuit taught by memory device of Kawamura into the memory device of AAPA for the purpose of providing a semiconductor memory having redundancy circuit which does not complicate the process of building in redundancy and which provides the access speed

comparable to the access speed for reading a normal memory cell (Kawamura, Col. 3 lines 12 – 17).

Allowed subject matter

7. Claims 6 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8.The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 6, in addition to other elements in the claim, the prior arts does not teach a memory device having one repeater between every two adjacent memory array blocks, wherein the repeater delays a control signal output from the RAS chain for a predetermined time and outputs the delayed control signal.

With respect to claim 8, in addition to other elements in the claim, the prior arts does not teach a memory device an output path of a first bit of the N bits of data is designed to output data faster than paths of output of data of next bits which are continuously output.

Prior art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Suh et al.	Patent No. 5,349,560	Date of Patent: Sep. 20, 1994
Song et al.	Pub. No. US 2002/0060938 A1	Pub. Date: May. 23, 2002

Contact Information

9. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (703) 305-1673. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Dang Nguyen 7/20/2004